WHAT IS CLAIMED IS:

1. In a substrate having an electrically nonconductive core with vias disposed therein and an electrically conductive reference layer formed on the electrically nonconductive core with voids in the electrically conductive reference layer that are formed around the vias in the electrically nonconductive core and electrically conductive traces on a routing layer overlying the electrically conductive reference layer, and a contact layer with electrically conductive contacts disposed in a contact pattern, the improvement comprising the core logically divided into sections, the vias within a given one of each of the sections aligned in rows substantially along a first direction and not aligned with the contact pattern, the voids in the reference layer within the given one of each of the sections also aligned in rows substantially along the first direction and aligned with the vias, and the traces within the given one of each of the sections also aligned substantially along the first direction between the rows of voids and not substantially overlying the rows of voids.

2. The substrate of claim 1, wherein the voids aligned within a given row are interconnected.

3. The substrate of claim 1, wherein the rows of vias within each of the sections of the core are all disposed in a same direction.

4. The substrate of claim 1, wherein the rows of vias within each of the sections of the core are not all disposed in a same direction.

5. The substrate of claim 1, wherein the first direction of the rows of vias within the given one of each of the sections is substantially disposed along a logical radial line from a center of the substrate.

6. The substrate of claim 1, wherein the reference layer is a power layer.

7. The substrate of claim 1, wherein the reference layer is a ground layer.

8. The substrate of claim 1, wherein the contacts on the contact layer are adapted for receiving ball bonds.

9. A packaged integrated circuit including the substrate of claim 1.

10. In a substrate having an electrically nonconductive core with vias disposed therein and an electrically conductive reference layer formed on the electrically nonconductive core with voids in the electrically conductive reference layer that are formed around the vias in the electrically nonconductive core and electrically conductive traces on a routing layer overlying the electrically conductive reference layer, and a contact layer with electrically conductive contacts disposed in a contact pattern, the improvement comprising the core logically divided into sections, the vias within a given one of each of the sections aligned in rows substantially along a first direction where at least a portion of the vias are not aligned with the contact pattern, the voids in the reference layer within the given one of each of the sections also aligned in rows substantially along the first direction and aligned with the vias, and the traces within the given one of each of the sections also aligned substantially along the first direction between the rows of voids and not substantially overlying the rows of voids.

11. The substrate of claim 10, wherein the voids aligned within a given row are interconnected.

12. The substrate of claim 10, wherein the rows of vias within each of the sections of the core are all disposed in a same direction.

13. The substrate of claim 10, wherein the rows of vias within each of the sections of the core are not all disposed in a same direction.

14. The substrate of claim 10, wherein the first direction of the rows of vias within the given one of each of the sections is substantially disposed along a logical radial line from a center of the substrate.

15. The substrate of claim 10, wherein the reference layer is a power layer.

16. The substrate of claim 10, wherein the reference layer is a ground layer.

17. A packaged integrated circuit including the substrate of claim 10.

18. In a printed circuit board having an electrically nonconductive core with vias disposed therein and an electrically conductive reference layer formed on the electrically nonconductive core with voids in the electrically conductive reference layer that are formed around the vias in the electrically nonconductive core and electrically conductive traces on a routing layer overlying the electrically conductive reference layer, and a contact layer with electrically conductive contacts disposed in a contact pattern, the improvement comprising the core logically divided into sections, the vias within a given one of each of the sections aligned in rows substantially along a first direction and not aligned with the contact pattern, the voids in the reference layer within the given one of each of the sections also aligned in rows substantially along the first direction and aligned with the vias, and the traces within the given one of each of the sections also aligned substantially along the first direction between the rows of voids and not substantially overlying the rows of voids.

19. The printed circuit board of claim 18, wherein the voids aligned within a given row are interconnected.

20. The printed circuit board of claim 18, wherein the rows of vias within each of the sections of the core are not all disposed in a same direction.